[0096] The thin film transistor Tr**1** includes the gate electrode Tr**1***g*, the second electrode Tr**1***s*, The first electrode Tr**1***d*, the oxide semiconductor layer **22**, and the insulating film **20**. The thin film transistor Tr**4** includes the gate electrode Tr**4***g*, the second electrode Tr**4***s*, The first electrode Tr**4***d*, the oxide semiconductor layer **22**, and the insulating film **20**.

[0097] The thin film transistor Tr**1** according to this embodiment has an offset gate structure in which the gate electrode Tr**1***g* is offset from the first electrode Tr**1***d* (first metal terminal) connected to the first wiring **3**. In contrast, the thin film transistor Tr**4** has an offset gate structure in which the gate electrode Tr**4***g* is offset from the first electrode Tr**4***d* (second metal terminal) connected to the second wiring **4**.

[0098] Specifically, the thin film transistor Tr**1** includes the first electrode Tr**1***d* (first metal terminal), the second electrode Tr**1***s* (third metal terminal), and an oxide semiconductor layer **22** that is provided at the upper surface side of the gate electrode Tr**1***g* with an insulating film **20** interposed therebetween.

[0099] The first electrode Tr**1***d* comes into contact with a first region **22**A, which is close to the first wiring **3**, in the upper surface of the oxide semiconductor layer **22**. The second electrode Tr**1***s* comes into contact with a second region **22**B, which is opposite to the first region **22**A, in the upper surface of the oxide semiconductor layer **22**. The gate electrode Tr**1***g* is separated from the first region **22**A so as to be offset in a direction from the first region **22**A to the second region **22**B of the oxide semiconductor layer **22**. The first region **22**A is also referred to as a source region or a drain region. The second region **22**B is also referred to as a drain region or a source region.

[0100] The thin film transistor Tr**4** includes the first electrode Tr**4***d* (second metal terminal), the second electrode Tr**4***s* (fourth metal terminal), and an oxide semiconductor layer **22** that is provided at the upper surface side of the gate electrode Tr**4***g* with an insulating film **20** interposed therebetween.

[0101] The first electrode Tr**4***d* comes into contact with a first region **22**A, which is close to the second wiring **4**, in the upper surface of the oxide semiconductor layer **22**. The second electrode Tr**4***s* comes into contact with a second region **22**B, which is opposite to the first region **22**A, in the upper surface of the oxide semiconductor layer **22**. The gate electrode Tr**4***g* is separated from the first region **22**A so as to be offset in a direction from the first region **22**A to the second region **22**B of the oxide semiconductor layer **22**.

[0102] In other words, in the thin film transistor Tr**1**, an end of the gate electrode Tr**1***g* which is close to the first electrode Tr**1***d* is arranged so as to be a predetermined distance x away from an end of the first electrode Tr**1***d* in a direction perpendicular to the laminated direction of the oxide semiconductor layer **22**. The end of the first electrode Tr**1***d* is an end of the first region **22**A where the first electrode Tr**1***d* is in contact with the oxide semiconductor layer **22**.

[0103] In the thin film transistor Tr**4**, an end of the gate electrode Tr**4***g* which is close to the first electrode Tr**4***d* is arranged so as to be the predetermined distance x away from an end of the first electrode Tr**4***d* in the direction perpendicular to the laminated direction of the oxide semiconductor layer **22**. The end of the first electrode Tr**4***d* is an end of the first region **22**A where the first electrode Tr**4***d* is in contact with the oxide semiconductor layer **22**. The first region **22**A is also referred to a third region, the second region **22**B is also referred to a forth region, in explaining the thin film transistor Tr**4**.

[0104] Next, the operation of the protection circuit **1**B according to the second embodiment will be described.

[0105] As described above, in the thin film transistor Tr**1**, a portion which is close to the first wiring **3** and is arranged in the vicinity of the first electrode Tr**1***d* is an offset gate. Therefore, when the voltage of the first wiring **3** connected to the first electrode Tr**1***d* is higher than the voltage of the second wiring **4**, current flows through the thin film transistor Tr**1**. On the other hand, when the voltage of the second wiring **4** connected to the second electrode Tr**1***s* is higher than the voltage of the first wiring **3**, no current flows through the thin film transistor Tr**1**.

[0106] In the thin film transistor Tr**4**, a portion which is close to the second wiring **4** and is arranged in the vicinity of the first electrode Tr**4***d* is an offset gate. Therefore, when the voltage of the second wiring **4** connected to the first electrode Tr**4***d* is higher than the voltage of the first wiring **3**, current flows through the thin film transistor Tr**4**. On the other hand, when the voltage of the first wiring **3** connected to the second electrode Tr**4***s* is higher than the voltage of the second wiring **4**, no current flows through the thin film transistor Tr**4**.

[0107] As such, in the protection circuit **1**B according to this embodiment, when the input voltage V_{IN} is positive with respect to the reference potential, the thin film transistors Tr**1**, Tr**2**, and Tr**3** prevent an overvoltage from being applied to an object to be protected. When the input voltage V_{IN} is negative with respect to the reference potential, the thin film transistors Tr**4**, Tr**5**, and Tr**6** prevent an overvoltage from being applied to the object to be protected.

[0108] FIG. **9** is a circuit diagram illustrating a modification example of the protection circuit **1**B according to the second embodiment. In the modification example illustrated in FIG. **9**, the thin film transistors Tr**1**, Tr**2**, and Tr**3** are p-channel transistors. Since the polarity of p-channel thin film transistors Tr**1**, Tr**2**, and Tr**3** are inverted to that of the n-channel transistor, their connection relationship between the electrodes is also inverted to that of the n-channel transistor.

[0109] FIG. **10** is a vertical cross-sectional view illustrating a modification example of the thin film transistors Tr**1** and Tr**4** with the offset gate structure according to the second embodiment. In the modification example illustrated in FIG. **10**, the thin film transistors Tr**1** and Tr**4** are a channel protection type and an insulating layer **21** that functions as a protective film is formed at the upper surface side of the oxide semiconductor layer **22**.

Third Embodiment

[0110] Hereinafter, a third embodiment will be described.

[0111] A thin film transistor Tr**1** and a thin film transistor Tr**4** according to this embodiment do not have an offset gate structure, as in the second embodiment. This is because a protection circuit **1**C controls line current, using both the thin film transistor Tr**1** and the thin film transistor Tr**4**, regardless of the polarity of an input voltage V_{IN}.

[0112] FIG. **11** is a circuit diagram illustrating the configuration of the protection circuit **1**C according to the third embodiment. In FIG. **11**, the same components as those in